CLAIMS

What is claimed is:

1. An method to transform a conditional state element, into a logically redundant element in a digital circuit design comprising:

coupling a first latency delay unit to a data input of the conditional state element;

coupling a second latency delay unit to an enable input of the conditional state element;

coupling a first input of a multiplexer to an output of the conditional state element;

coupling a second input of the multiplexer to the data input of the conditional state element; and

coupling a select line of the multiplexer to the enable input of the conditional state element.

2. The method of claim 1 wherein coupling a first latency delay unit to a data input of the conditional state element comprises coupling a signal with a delay of one unit into the data input of the conditional state element.

3. The method of claim 1 wherein coupling a second latency delay unit to an enable input of the conditional state element comprises coupling a signal with a delay of one unit into the data input of the conditional state element.

4. The method of claim 1 further comprising replacing the conditional state element in a finite state machine with the logically redundant element said finite state machine having an F function and a G function, coupled to the logically redundant element.

5. The method of claim 1 wherein transforming a conditional state element, into a logically redundant element in a digital circuit design comprises transforming any one of a flip-flop, a register file, and a deterministic memory into a logically redundant element.

6. The method of claim 4 wherein replacing the conditional state element in a finite state machine with the logically redundant element comprises:

coupling the first latency delay unit to an output of the F function;

coupling the second latency delay unit to an output of the G function; and

coupling the multiplexer output to an input of the F function, and to an input of the G function.

7. The method of claim 6 further comprising:

adding a first –1 latency delay unit to a latency delay unit coupled to the output of the finite state machine, said latency delay unit not in a feedback loop of the finite state machine;

adding a +1 latency delay unit and a second –1 latency delay unit between the output of the finite state machine and the data input of the conditional state element;

eliminating latency delay units by any one of reduction of the latency delay units and rerouting of the first input of the multiplexer, to automatically create a bypass logic circuit to the finite state machine.

8. An apparatus to transform a conditional state element, into a logically redundant element in a digital circuit design comprising:

a memory;

a processor; and

a bus coupled to the memory and the processor, the processor to

identify a conditional state element;

couple a first latency delay unit to a data input of the conditional state element;

couple a second latency delay unit to an enable input of the conditional state element;

couple a first input of a multiplexer to an output of the conditional state element;

couple a second input of the multiplexer to the data input of the conditional state element; and

couple a select line of the multiplexer to the enable input of the conditional state element.

9. The apparatus of claim 8 wherein the conditional state element further comprises at least one of a flip-flop, a register file, and a deterministic memory.

10. The apparatus of claim 8 wherein the processor to couple a first latency delay unit to a data input of the conditional state element comprises the processor to couple a signal with a delay of one unit into the data input of the conditional state element.

11. The apparatus of claim 8 wherein the processor to couple a second latency delay unit to an enable input of the conditional state element comprises the processor to couple a signal with a delay of one unit into the data input of the conditional state element.

12. The apparatus of claim 8 further comprising the processor to replace the conditional state element in a finite state machine said finite state machine having an F function and a G function coupled to the logically redundant element.

13. The apparatus of claim 12 wherein the processor to replace the conditional state element in a finite state machine with the logically redundant element comprises the processor to:

couple the first latency delay unit to an output of the F function;

couple the second latency delay unit to an output of the G function; and

couple the multiplexer output to an input of the F function, and to an input of the G function.

14. The apparatus of claim 13 further comprising the processor to

add a first –1 latency delay unit to a latency delay unit coupled to the output of the finite state machine, said latency delay unit not in a feedback loop of the finite state machine;

add a +1 latency delay unit and a second –1 latency delay unit between the output of the finite state machine and the data input of the conditional state element;

eliminate latency delay units by any one of reduction of the latency delay units and rerouting of the first input of the multiplexer, to automatically create a bypass logic circuit to the finite state machine.

15. An article of manufacture to transform a conditional state element, into a logically redundant element in a digital circuit design comprising:

a machine-accessible medium including instructions that, when executed by a machine, causes the machine to perform operations comprising

identifying a conditional state element;

coupling a first latency delay unit to a data input of the conditional state element;

coupling a second latency delay unit to an enable input of the conditional state element;

coupling a first input of a multiplexer to an output of the conditional state element;

coupling a second input of the multiplexer to the data input of the conditional state element; and

coupling a select line of the multiplexer to the enable input of the conditional state element.

16. The article of manufacture of claim 15 wherein said instructions for coupling a first latency delay unit to a data input of the conditional state element comprises further instructions for coupling a signal with a delay of one unit into the data input of the conditional state element.

17. The article of manufacture of claim 15 wherein said instructions for coupling a second latency delay unit to an enable input of the conditional state element comprises further instructions for coupling a signal with a delay of one unit into the data input of the conditional state element.

18. The article of manufacture of claim 15 further comprising instructions for replacing the conditional state element in a finite state machine with the logically redundant element said finite state machine having an F function and a G function, coupled to the logically redundant element.

19. The article of manufacture of claim 18 wherein said instructions for replacing the conditional state element in a finite state machine with the logically redundant element comprises further instructions for:

coupling the first latency delay unit to an output of the F function;

coupling the second latency delay unit to an output of the G function; and

coupling the multiplexer output to an input of the F function, and to an input of the G function.

20. The article of manufacture of claim 19 comprising further instructions for

adding a first –1 latency delay unit to a latency delay unit coupled to the output of the finite state machine, said latency delay unit not in a feedback loop of the finite state machine;

adding a +1 latency delay unit and a second –1 latency delay unit between the output of the finite state machine and the data input of the conditional state element;

eliminating latency delay units by any one of reduction of the latency delay units and rerouting of the first input of the multiplexer, to automatically create a bypass logic circuit to the finite state machine.